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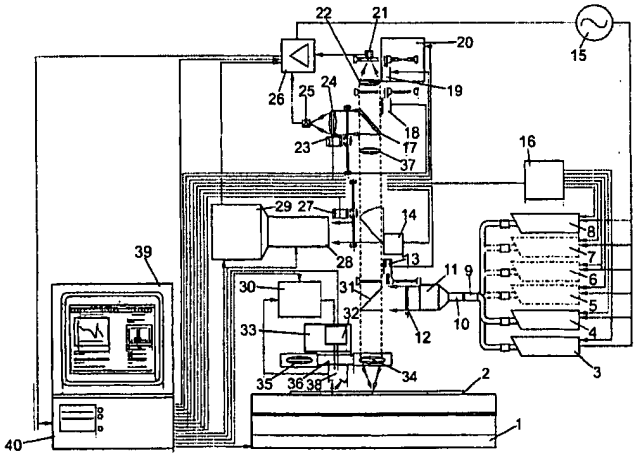

(57) Abstract: A method of quality screening silicon germanium epilayers by measuring defects and contamination therein comprises the growing a silicon germanium layer epitaxially, for example by chemical vapour deposition, on a suitable substrate, for example a semiconductor structure such as a silicon wafer; exposing the surface of the silicon germanium layer to at least one high-intensity beam of light from a suitable light source, preferably a laser, and in particular a high-intensity laser, and collecting photoluminescence (PL) produced by excitation of the silicon germanium layer by the light beam; numerically analysing the photoluminescence emitted across the area of the structure; comparing the result with a predetermined acceptable specification range of photoluminescence; making a quality classification of the silicon germanium layer structure based thereon, and in particular rejecting or selecting for remedial action grown silicon germanium layers exhibiting a photoluminescence response outside the said predetermined acceptable specification range. An apparatus for performing the method, and such an apparatus incorporated into a SiGe growth reactor, are also described.

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DETECTION METHOD AND APPARATUS

The invention relates to a non-destructive method and apparatus for detecting surface layer metal contamination and defects in silicon germanium semiconductor structures. The invention in particular provides for an improved quality control metric for the processing and fabrication of silicon germanium based devices.

The increasing demand for multimedia transmission through wired and wireless communications has resulted in the need for higher operating frequencies and bandwidth. Silicon germanium (SiGe) has intrinsic electrical properties that enable advantages over silicon, such as higher frequency operation and improved signal reception and greater power efficiency. Band gap engineering can be used to create SiGe structures optimized for speed or power in a given device application.

SiGe ICs are fabricated on Si substrates; a small amount of Ge is then added to the transistor structure extending the device performance. Processing SiGe on existing Si fabrication lines means that SiGe chips benefit from the reduced cost per chip. Also the advantages of complementary metal oxide semiconductor devices (CMOS) can be mixed directly with SiGe heterojunction bipolar technology into a new process (BiCMOS).

A thin layer of SiGe can be grown on a Si substrate by an epitaxial process, for example using a chemical vapour deposition (CVD) epitaxial reactor. The SiGe layer will adopt the lattice spacing of the underlying Si if the layer is kept thin (<10 nm) and the composition is low (<15%). The compressive stress produced in the SiGe layer improves the hole mobility and the emitter-base band offset markedly increasing the operating frequency of a SiGe based

device. A strained Si layer grown on a relaxed SiGe layer causes the electron mobility to increase, increasing the frequency of a CMOS device.

When growing epitaxial films of germanium (Ge has a 4.2% larger lattice constant than Si) or the alloy SiGe on a silicon substrate, there exists a maximum thickness, above which it is difficult to maintain a strained layer in coherence with underlying Si lattice spacing. Then defects are produced, in this case misfit dislocations, which act to relieve the strain in the epitaxial film. The epitaxial layer is said to relax and the defects significantly reduce the mobility and electronic quality of the material. Heterogeneous defect formation can occur in strained layers, due to incomplete surface cleaning or contamination during growth. Also SiGe contamination can occur from the susceptor (used to heat the wafer), or from poor surface cleaning prior to growth.

Defect analysis is usually carried out on SiGe wafers using wet chemical etching; this technique is destructive and very slow. This method also involves the handling of dangerous chemicals, which means an experienced operator is required and there are high costs for chemical waste disposal. Laser surface scanning methods (using scattered light imaging) used to detect surface particles are sometimes also applied to detecting imperfections in SiGe wafers. Some defects in SiGe create changes in the surface topography and can therefore be detected because they scatter light. However this method will not work on pattered wafers used for device fabrication.

The standard method for measuring surface metal contamination is total x-ray reflection fluorescence (TXRF). This technique can determine the type of contamination and the concentration. However, this technique has no wafer mapping capability and takes approximately one hour to make one measurement covering a 1 cm^2. Also this technique is usually based outside

the clean room area and it takes time to get the results due to the intensive demand.

There is a metrology requirement for whole wafer mapping to measure defects and contamination in SiGe wafers. With rapid measurement an indication of the layer quality can be obtained quickly, and this information can be used to optimize the growth conditions and identify any sources of contamination in the reactor. Regular wafer scanning will give fast feedback on the wafer quality and can eliminate the number of wafers lost due to misprocessing and boost device yield. In addition, the preventative maintenance schedule can be carried out more cost effectively, by detecting defects early using wafer scanning.

It is an object of the present invention to provide a method and apparatus for measuring defects and contamination in SiGe wafers which mitigates some or all of the above disadvantages.

It is a particular object of the present invention to provide a method and apparatus which gives an accurate indication of epilayer quality at enhanced throughput rates.

It is a particular object of the present invention to provide a method and apparatus which gives an accurate scan of epilayer quality which can be spatially resolved across a test sample.

Thus, in accordance with the present invention in its first aspect a method of quality screening silicon germanium epilayers by measuring defects and contamination therein comprises the steps of:

growing a silicon germanium layer epitaxially, for example by chemical vapour deposition, on a suitable substrate, for example a semiconductor structure such as a silicon wafer;

exposing the surface of the silicon germanium layer to at least one high-intensity beam of light from a suitable light source, preferably a laser, and in particular a high-intensity laser, and collecting photoluminescence (PL) produced by excitation of the silicon germanium layer by the light beam;

making an analysis of the collected photoluminescence signal and using that analysis as the basis for a quality classification of the suitability of the semiconductor for further processing.

The quality classification step comprises performing a numerical analysis of the collected photoluminescence signal, comparing the result of that numerical analysis with a predetermined acceptable photoluminescence specification such as a predetermined range of photoluminescence known to be associated with satisfactory quality, and making a quality classification of the semiconductor structure based thereon.

In one simple alternative the numerical analysis can comprise a simple defect count, with the aggregate result being compared with a predetermined limit. It might often be preferably if a method taking a representative measure from on or more areas is used. For example the method comprises determining an average photoluminescence intensity over the whole area or a series of subregions, comparing the average with a predetermined acceptable specification range of photoluminescence, and making a quality classification of the semiconductor structure as above based thereon.

The average may be a whole area average based on mean photoluminescence intensity emitted across the area of the structure, or local area average wherein the area of the structure is divided into a two dimensional array of subregions,

a mean photoluminescence intensity is determined for each subregion, the mean for each subregion is compared with a predetermined acceptable photoluminescence specification, and a quality classification as above is based thereon. This can be advantageous since the response attributable to an isolated defect could be swamped in a whole area average even though that defect was sufficiently serious to justify a quality rejection. At an appropriate subregion size it is possible to ensure that such a response can still be detected.

Use of a predetermined photoluminescence specification based on the mean is an example only. In the alternative, especially if the subregion approach is followed, other numerical parameters could be applied to the analysis of the photoluminescence signal, such as standard deviation, local maxima and/or minima, deviation from a predetermined baseline, or other numerical analysis method to determine, either on a local or whole area basis, a deviation of the photoluminescence response from predetermined parameters known to be associated with a semiconductor structure of satisfactory quality. Where reference is made below to numerical analysis based on average luminescence it will be appreciated that this is for exemplification only and that the precise numerical parameters chosen for the comparison between observed and predetermined acceptable response is not critical to the invention.

The photoluminescence technique can be used to detect both defects in the epilayer such as might arise as structural defects such as misfit dislocations, or as heterogeneous defects in strained layers, due to incomplete surface cleaning or contamination prior to or during growth. It is thus an admirable technique for detecting many of the defects likely to have an adverse effect on SiGe device performance.

The photoluminescence technique produces a much more rapid response than prior art TXRF techniques. In its preferred basic form described above it

samples across the whole wafer area and produces an average result based upon that whole wafer. This is surprisingly found to give an effective and representative quality control metric allowing for rapid testing of successively produced structures as part of a production process. The speed and accuracy of the technique make it a much more effective and practical quality control method than prior art techniques.

In a preferred further aspect the invention thus comprises a quality control metric for silicon germanium epilayers intended for device fabrication thereupon, comprising the successive monitoring of a successive series of grown layers in the manner above described, passing a layer exhibiting a photoluminescence response within the predetermined acceptable specification range of photoluminescence onto the next device fabrication stage, rejecting a layer exhibiting a photoluminescence response outside the predetermined acceptable specification range of photoluminescence from the next device fabrication stage, for example passing such a structure for remedial treatment or rejection.

In accordance with this preferred aspect all grown layers may be tested and quality screened prior to device fabrication. Potential problems are identified early, prior to expensive fabrication processes. The number of rejects necessary at the end of fabrication should be reduced significantly since the method of the invention enables accurate diagnosis and rejection of poor quality layer structures prior to device fabrication in a rapid and convenient manner.

The photoluminescence technique produces a spatially resolved PL map at a resolution determined by the characteristics of the high-intensity beam of light. This can be exploited by further preferred features of the present method, but for the fundamental objective of the invention as a simple and

rapid quality test for a grown epilayer an average PL intensity result over the whole layer area is obtained. This can be related to a predetermined acceptable specification range developed in association with studies using slower analysis methods (eg TXRF). It has been surprisingly found, as described in detail below, that a close correlation can be demonstrated between defect data obtained from the layer using the PL technique of the present invention and prior art methods conventionally used.

The light beam is so controlled, and in particular beam power and/or wavelength and/or spot size so controlled, as to identify defects and contamination at a selective depth in said semiconductor structure, so as to collect PL information from a suitable at- or near-surface depth, for example from the upper 12 μm of the semiconductor structure. For certain materials and devices, smaller depths may be appropriate, down to for example 5 μm or even 1 μm.

The present invention is a defect and contamination monitoring tool that can be used to monitor contamination and other structural defects such as misfit disclocations in the grown layer. Because this technique measures the surface region it will detect defects and contamination within the epilayer accurately. These defects are most determinative in their impact on device quality and performance. This further enhances the accuracy and reliability of the technique. Moreover, there are some important defect types (such as threading dislocations or sub-surface detects) that the laser surface scanning methods cannot detect which can be detected by the present invention. There is also the added benefit that the present invention can be used to detect defects on patterned wafers.

In accordance with the invention in its preferred basic embodiment, a predetermined acceptable specification range of average photoluminescence is

first determined and then used as a reference for the results for any given as-cleaned wafer for quality control purposes. The predetermined specification range will include a minimum and/or maximum photoluminescence value. In particular, it is known that the photoluminescence signal can be affected in different ways depending upon the particular chemical species comprised in the impurity. Accordingly, the specification range will preferably comprise a minimum and a maximum photoluminescence value.

A quality control decision is taken depending upon whether the measured result lies within the predetermined specification range to accept structures for device fabrication when within the range, and to reject when outside the range. Rejected items may be discarded or subjected to remedial. For example the base structure may be recycled and a further epilayer grown thereon and then tested as above. The predetermined acceptable PL range will vary in accordance with the particular material and process involved and will be determined initially from existing quality control specification ranges by relating the PL responses produced by the present invention with responses in accordance with existing prior art measuring techniques.

Once such a specification range has been established, the present invention provides very high throughput relative to prior art methods. For example, for a 12 inch (300 mm) wafer equivalent results can be obtained in around five minutes that would take around an hour with existing methods.

Photoluminescence spectroscopy is a very sensitive technique for investigating both intrinsic and extrinsic electronic transitions at impurities and defects in semiconductors. When the semiconductor is excited at low temperatures with laser irradiation above the band-gap of the material, electron hole pairs are produced. These carriers can recombine in various different ways, some of which give rise to luminescence. The electron hole pairs formed at low

temperature can be trapped at impurities in the layer and they emit photons characteristic of this interaction, thereby giving impurity specific information in the photoluminescence spectra. There are a significant number of applications of PL spectroscopy to semiconductors including characterisation of the material after different processing steps, characteristic of device fabrication for example implantation, oxidation, plasma etching, the detection of point defect complexes and the presence of dislocations. One of the most important applications includes the non-destructive measurement of shallow donors and acceptors such as arsenic, boron and phosphorous. Notably, this technique enables the measurement of the concentration of these shallow donors and acceptors. However, in conventional applications in order to obtain this spectral information and unambiguous chemical identification of the optical centres, measurements need to be carried out at liquid helium temperatures. It is known throughout the industry that at room temperature the PL signal is significantly weakened and very little useful spectral information can be obtained.

A room temperature technique is accordingly preferred, such as in particular that described by International patent application WO98/11425, which describes a non-destructive technique which makes practical the detection of electrically active defects in semi-conductor structures based on room temperature PL. The patent application discloses a PL technique which has industrial application in that it enables the image to be produced within minutes and which has a further added advantage in producing micro imaging of small individual defects particularly near to the surface of the wafer, where the device is fabricated. The technique provides information concerning defects in a semiconductor or silicon structure at a rate appropriate to industrial use and in particular enables us to visualise defects in the upper regions of the semiconductor or silicon structure and in particular near to the surface of same.

The technique exploits enhanced non-radiative recombination of electron hole pairs at defects in a semiconductor or silicon structure with a view to enhancing contrast in a PL image of said semiconductor or silicon structure so as to enhance the viewing of defects in same. The preferred PL technique for use in the present invention is therefore that in WO98/11425, incorporated herein by reference.

The use of this technique to characterise certain defects in silicon germanium epilayers is briefly considered in V. Higgs, Mat. Res. Soc. Symp. Proc. **Vol. 588**, 129, 2000. However, the present invention exploits the fact that it is not necessary to characterise in detail the type or position of impurities in the structure. Instead, a simple, rapid but surprisingly effective quality metrology for the control and monitoring of the SiGe growth process can be obtained by the method of the invention.

The success of the room temperature PL method disclosed in the reference is, in part, due to the probing volume probed by the laser being small, spatial resolution preferably 0.1 to 20 μm, ideally 2 to 5 μm, and with a peak or average power density of between 10^4 to 10^9 watts/cm^2, so that localized defects have much greater effect on the measured PL intensity and is also believed, in part, because since the excitation is focused the injected carrier density is high. This greatly increases the probability of non-radiated recombination at the defect and hence physical location of the defect. The present invention in certain preferred embodiments described in more detail below exploits this by preparing a spatial map, and more preferably still a spatial image, of the defects of which the PL response is representative.

Reference herein to a high-intensity laser is meant to include, without limitation, a high power density laser i.e. where regardless of the power of the laser the emittance is focused.

In a preferred method of the invention a pulsed laser excitation source is used and ideally luminescence data is measured and/or the luminescence images collected as a function of time. This means that both depth and spatial resolution are improved and can be used to obtain information on the carrier capture cross sections of the defects. Time resolved measurements can also be used to measure the effective carrier lifetime and obtain lifetime maps.

The PL technique of the present invention generates a spatially resolved PL map across the area of the wafer. In the primary method of the invention, this data map is then processed to provide an average PL level across the whole wafer, which is compared with the reference to make the quality control decision. If the method is to be used for a simple accept/ reject and reclean quality control decision as a test prior to passing structures on for the next stage of manufacture then only the averaged PL level is of concern, and the resolution of the map produced by the method is immaterial. Resolutions of the order of 2-7 mm are adequate. At this level of resolution, processing times are reduced, and test throughput rates maximized. For example it can take just five minutes to obtain a satisfactory accept/ reject result from a 12 inch (300 mm) wafer.

Nevertheless, it is a particular advantage of the preferred photoluminescence technique of the present invention that it can additionally be used to generate a spatially resolved map of PL signals across the surface of the semiconductor structure under test, and in particular to generate a spatially resolved image of those signals. Such a spatially resolved map is simply not practical over practical timescales with prior art TXRF techniques. Accordingly, in a

preferred embodiment, the method further comprises the step of generating such a map and/or such an image. In these circumstances, it can be appropriate to work to mapping/imaging resolutions of 0.5 mm or less.

Conveniently, the method further comprises storing the spatially resolved PL map on suitable data storage means and/or transmitting digitized data derived from the spatially resolved map through suitable processing means for onward processing and/or displaying the spatially resolved image on suitable display means.

The basic technique identifies an averaged PL intensity on which to base the accept/ reject or reclean decision. Spatially resolved information is especially useful in relation to rejected structures. A preferred more developed quality control strategy might therefore be to process each unit using the more rapid, basic technique, and to generate spatially resolved data for rejected structures only. In one embodiment, taking full advantage of the ability of the technique to produce spatially resolved data on the PL response of a semiconductor structure under test, it might be appropriate, as indicated, to work at higher resolutions. Accordingly, throughput will be slower than where the technique is used as a basis for basic accept/ reject quality control decisions only. A preferred more developed quality control strategy might therefore be to process each unit using the more rapid, basic technique, and to reprocess rejected structures at higher resolution using the additional functionality offered by the collection of spatially resolved data.

The ability to generate a map or image allows defect location to be generally identified. This can be exploited in a preferred embodiment of the invention in that the method as hereinbefore described can be used to rapidly screen layer structures (5 minutes for a 300 mm wafer) and identify specimens for a full defect analysis. This embodiment of the method comprises subjecting a

silicon germanium layer to the test as hereinbefore described to generate a spatially resolved map of PL signals across the surface of the layer structure an, at least in the case of rejected structures, using the spatially resolved map to identify the general location of defects, and further analysing the layer in the identified location using a specific analysis technique capable of characterising the defect. For example, a micro scan may be carried out on the layer to reveal individual stacking faults and like structural defects.

In accordance with a further aspect of the invention an apparatus for quality screening silicon germanium epilayers by measuring defects and contamination therein comprises a test device comprising a high intensity light source, preferably a laser, and in particular a high-intensity laser; means to focus a high intensity beam of light from the light source onto a surface of the silicon germanium layer under test; collection means to collect photoluminescence data from across the surface of the layer under test produced by excitation of the semiconductor structure by the light beam; analysis means to process and numerically analyse the collected data; a comparator to compare the results of the analysis with predetermined acceptable specification parameters, and to accept or reject the structure determined by whether the photoluminescence signal falls within the predetermined acceptable specification range.

More preferably, the apparatus comprises a means to grow an epitaxial silicon germanium layer on a suitable substrate, such as a chemical vapour deposition epitaxial reactor, in conjunction with a test device as above to test the as grown silicon germanium layer. Transfer means may be provided to sequentially transfer grown layers from the reactor to the test device as part of a process control system.

The apparatus may form part of a production line and include transfer means adapted to transfer the structure to a particular further processing stage determined by whether the photoluminescence signal falls within the predetermined acceptable specification range.

In particular the transfer means is adapted to transfer a structure exhibiting a photoluminescence response within the predetermined acceptable specification range of photoluminescence on to the next device fabrication stage, and to reject a structure exhibiting a photoluminescence response outside the predetermined acceptable specification range of photoluminescence.

The apparatus to perform the basic method generates data based on a numerical analysis of the PL response, for example an average PL signal across the whole area or a set of local area data as described. This is compared with predetermined acceptable specification parameters.

However, to perform the refined alternatives of the method described above, the apparatus preferably further comprises means to resolve the collected PL data into a spatially resolved PL map across the area of the semiconductor structure, and optionally further comprises means to convert the resolved data into a PL image and/or image/data storage means to store the map/image, and in particular to store successive map/images for future comparison, and/or means to transmit the map/image to a suitable remote data processor and/or image display means such as a visual display screen to display an image and/or related data to a user. The apparatus may further be provided in association with a micro scanner to characterise defects spatially identified by the PL map. Other preferred apparatus features will be understood by analogy with the method.

In a further aspect of the invention, there is provided a computer program and/or a suitably programmed computer for performing some or all of the steps of the method as hereinbefore described, and in particular for performing data processing steps on collected PL data, for example to determine average PL across the wafer area and/or to spatially resolve a PL map from collected PL data and/or to compare the average with a predetermined acceptable specification range.

The invention will now be described by way of example only with reference to Figures 1 to 11 of the accompanying drawings in which:

Figure 1 is an illustration of a suitable apparatus for obtaining the PL data;

Figure 2 is a schematic illustration of how data is processed;

Figure 3a is a wafer map revealing areas of contamination (with a higher PL value than average and Figure 3b is a micro scan of the wafer revealing individual stacking fault defects (scan area 3 x 6 mm);

Figure 4a is a further wafer map revealing areas of contamination (with a higher PL value than average and Figure 4b is a micro scan of the wafer revealing individual stacking fault defects (scan area 9 x 11 mm);

Figure 5a is a further wafer map revealing misfit dislocations and Figure 5b is a micro scan of the wafer showing the defects more clearly (4 x 3 mm);

Figure 6a-d are wafer front surface and backside comparisons;

Figure 7 is a micro map revealing features attributed to threading dislocations (0.35 x 0.29 mm);

Figure 8 illustrates correlation of PL data to a basic quality control accept/ reject decision;

Figure 9 illustrates a spatially resolved PL image of a wafer;

Figures 10 and 11 illustrate a possible numerical analysis technique in accordance with the invention.

The apparatus illustrated in Figure 1 essentially comprises a PL imaging microscope which: towards the right hand side, comprises a bank of lasers (3-8); towards the bottom comprises a sample stage such as an X-Y table or R-table; towards the left hand side comprises a microprocessor (40) and a display screen (39) and in the centre of the figure there are shown various optical components for directing light through the system.

In the embodiment shown in Figure 1, six lasers are provided with a view to probing different depths in the sample. However, it is within the scope of the invention to use only one laser, or indeed to use a greater number of lasers. In any event, at least one of the lasers is a high intensity laser and ideally has a spot size of between 0.1 mm and 0.5 micron and a power density of between 10^4 to 10^9 watts/cm^2. A laser selector (16) coupled with said bank of lasers is provided so as to select one or more lasers for use and further also to select the frequency and wavelength of the lasers.

Conventional optics, such as optical fibres (9) are used to direct light towards the collimator to (10) and laser beam expander (11). An apodization plate (12) is positioned between laser beam expander (11) and beam splitter (31). Beam splitter (31) directs a fraction of light from the aforementioned lasers towards sample (2) via objective (34).

An automatic focus controller (30) is provided and coupled to a piezo driven focusing stage (33). The microscope is equipped with a conventional rotating turret (36) which is provided with at least one high numerical aperture objective for micro examination and one low numerical aperture objective for macro examination (34, 35) respectively. In addition, also coupled to turret (36) there is provided an optical displacement measuring system (38).

Cabling is provided so as to connect the automatic focusing controller (30) to microprocessor (40) and also a microscope objective indexing arrangement (32) to microprocessor (40).

Downstream of beam splitter (31) there is provided as filter wheel (13) for laser notch filters, down stream thereof there is provided a swing-aside folding mirror (14) whose function will be described hereinafter. Aligned with said mirror (14) there is provided a filter wheel (27) for wavelength selection, and rearward thereof there is provided a zoom lenses attached to a suitable CCD 2-D array detector (29).

Infinity system compensating lens (37) is provided in the optical path foremost of cold mirror (17) which reflects light towards a further filter wheel (23) for wavelength selection and a focusing lenses (24) which is foremost of a detector (25) for UV and visible light. Detector (25) is coupled to lock-in amplifier (26). This is used to obtain a reflected image of the surfaces.

Rearmost of cold mirror (17) is provided a further filter wheel (18) again for wavelength selection, and rearmost thereof a focusing lens (22) and a further aperture wheel (19) for pinhole selection which is provided foremost of a detector (21) for detecting the luminescence.

Both the UV and visible region detector (25) and infrared detector (21) are coupled to lock-in amplifier (26).

Operation of the system is explained having regard to the following.

A range of wavelengths to probe different planes in the sample is provided by several lasers (3-8). The lasers can be modulated by a frequency generator (16) so that the signal emitted from the sample (2) can be isolated from background radiation by means of the detectors being synchronised to the laser modulation frequency by the lock-in amplifier (26). In a further embodiment, the range of wavelengths could be produced by using a tuneable laser and/or an Optical Parametric Oscillator. Each laser is connected to, and aligned with, a Multi-branch optical fibre (9) so that any or all of the lasers can illuminate the sample (2). The common end of the Multi-branch optical fibre terminates in an optical system (10) which collimates the emerging light. This optical system is aligned with a beam expander (11) which matches the laser beam's diameter to that required by the microscope objectives (34,35) above the sample (2). The expanded beam then passes through an apodization plate (12) which distributes the optical energy evenly over the beam area.

The expanded and apodized beam is reflected by a beamsplitter (31) and passes to the microscope objectives (34 and 35). The beam is focused by a microscope objective (34 or 35) on to the sample. In the micro mode this objective is selected to focus the beam to a diffraction limited spot size. A rotating turret (36), operated by an indexing mechanism (32), permits the objective to be changed for the macro mode where a larger area of the sample can be illuminated. In a further embodiment the apodization plate (12) can be removed so that the spot for the micro mode can be made smaller to allow higher injection levels.

An optical displacement sensor (38) measures the distance to the sample and, by means of a feedback loop through the autofocus controller (30), maintains the correct spacing by means of the piezo actuated focusing stage (33).

The Photoluminescence signal from the sample is collected by the microscope objective (34) (in the micro mode) and transported back through the beamsplitter (31) and a notch filter in the filter wheel (13) which contains notch filters matched to the range of laser wavelengths. The notch filter removes any reflected laser light, passing only the Photoluminescence signal.

The folding mirror (14) is swung out of the beam allowing the signal to pass to the tube lens (37), which may be incorporated to compensate for any infinity microscope objectives which may be used, and on to the cold mirror (17). This component reflects those wavelengths below a selected cut off point (approximately 700 nm) to the focusing lens (24) which focuses the signal into the detector (25). A filter wheel (23) in front of the detector focusing lens (24) contains filters to isolate selected wavelength bands.

The portion of the Photoluminescence signal lying in the wavelength range above the cut-off point passes through the cold mirror (17) and is similarly focused by the lens (22) into the detector (21). This signal also passes through a filter wheel (18) containing filters to isolate selected wavelength bands.

A series of pinholes of different diameters are contained in an aperture wheel (19) positioned in front of the detector (21). This aperture wheel can be moved axially by the piezo actuator (20) so that the pinholes can be positioned confocally with the desired image plane. By this means, planes at different depths in the sample (2) can be imaged to provide accurate depths information.

The electrical signal from the detectors (21, 25) is fed to the lock-in amplifier (26) where it is synchronised with the modulation frequency of the laser (3-8) by means of a reference signal from the frequency generator (15). The electric signal is then fed to the central processor (40) for analysis. The PL image is obtained by raster scanning the stage. Alternatively optical scanning using galvo mirrors may be employed.

In an alternative micro mode of operation, the folding mirror (14) is swung into the beam of the Photoluminescence signal. The diverted signal passes through a filter wheel (27), which contains filters to isolate selected wavelength bands, and into the zoom lens (28). The zoom lens allows different magnifications to be used in imaging the illuminated spot on the sample (2) on to the CCD two dimensional array (29). This allows the illuminated area of the sample (2) to be imaged at different resolutions. The electrical signal from the CCD array is fed to the central processor (40) for analysis.

The processing of data is illustrated schematically in Figure 2. A sample (101) comprising a suitable substrate on which a silicon germanium epitaxial layer has been grown in the a chemical vapour deposition epitaxial reactor (100) is transferred by a handling arm (102) onto a sampling base (103) for testing by the device of Figure 1 to generate a PL signal. This is collected by the collection apparatus of Figure 1 (shown in simplified schematic form as the device 105).

The figure further illustrates processing of data. In a first processing path, in accordance with the main aspect of the invention, the PL map data is passed to a processor (107) which processes the data to determine an average PL intensity across the whole area of the sample (101).

The resulting average is passed to a comparator (108) which relates the average PL intensity data to a predetermined stored specification range within the data store (109), and based on that comparison passes a quality control decision onto the control unit (110). In the embodiment the control unit (110) acts directly upon the handling arm (102) which then transfers the sample (101) on to a device fabrication processing line or to a reject line for remedial action or discard. In an alternative mode of operation, the control unit (110) could for example be a display means giving an indication to an operator, who could then operate the arm (102) by separate control means for example to make an acceptable/reject choice, to divert the sample under test for remedial processing etc.

A secondary processing route, shown by the broken line, reflects the optional second aspect of the invention. In this optional aspect, data corresponding to the PL intensity map across the surface of the sample (101) is also passed to a secondary processing unit (111) which is able to resolve the data into a digitised spatially resolved map of intensity across the surface of the sample (101). The resulting map is passed to a data store (112) and to a visual display screen (113). The resolved data may be used to identify defect locations. In this way the basic apparatus could be used to rapidly screen wafers. The location of contamination may be identified from the wafer map, and then the wafers could be further analysed using micro scanning or other techniques to characterise the defects.

To illustrate that the technique could be used to monitor SiGe wafer quality and optimize the growth conditions, a selection of different 200 mm wafers were measured grown under different conditions. After analysis of the wafers and inspection of the wafer maps, it was clear that some of the wafers revealed a common feature. An example of this type of contamination is shown in Figure 3a. There were areas on this wafer that had a much higher value of PL

signal compared to the average background level (White marks in Figure 3a). This exact area was measured using TXRF and showed that this was due to Cu contamination. This supports the idea that Average PL can be used as a metric to determine the wafer quality in terms of contamination. A micro scan was recorded at this location and the PL scans revealed small stacking faults defects, this was confirmed by inspection of the same location using optical microscopy.

A second common defect feature was revealed in the wafer maps and this area was also analysed, the corresponding wafer map is shown in Figure 4a. This wafer contained localised areas of reduced PL (show as dark spots in the wafer map) below the average value for this wafer. These dark areas were further investigated using high-resolution micro scans. The image obtained from scanning one of the locations is shown in Figure 4b. This feature is a defect (surface particle of contamination) that caused the nucleation of misfit dislocations. The results shown obtained clearly suggest that the wafer maps can used to determine the presence of contamination or defects. Then areas of interest can be re-scanned at higher resolution to reveal the identity of the defect type.

To investigate further how the technique could be used to monitor the SiGe growth process, a number of 200 mm wafers were grown at the same temperature, but the pre-growth cleaning annealing temperature was varied. This pre-growth anneal is used to remove contamination and any residual surface oxide. Each wafer was measured and the defect quality determined using a micro scan. The same wafers were also measured using a laser surface scanning method. The defect density determined by both techniques is shown in the table below.

Pre-Growth Clean Temperature	SiPHER Defects density (Defects/cm^2)	Laser Surface scanner (Defects/cm^2)
Low	3000	2000
Medium	10-20	10-20
High	<1	1.5

There is a good correlation in terms of the defect density, and the results show that the defect density decreases as the pre-growth anneal temperature increases. This result is consistent with defect etching studies, that the low temperature anneal does clean the surface effectively and more defects are formed during SiGe layer growth.

These results support the idea that the room temperature PL apparatus of Figure 1 can be used to detect defects in SiGe and the results can be processed in accordance with the Figure 2 procedure and used for process optimization. The apparatus can detect some important defect types (such as threading dislocations or sub-surface detects) that laser surface scanning methods cannot. The apparatus can also be used to detect defects on patterned wafers.

An additional function that can be carried out by the technique is to review the source of front side contamination inspecting both sides of the wafer. Front side contamination can be created by backside contamination or damage prior to SiGe growth. Then after SiGe growth defects can propagate to the front side or contamination diffuses to the front side. An example of this type of problem is shown in Figures 5 and 6. The wafer map contained defect areas (areas of lower than average PL intensity) labelled "A" and "B" in Figure 5a. A micro scan shows the defects at position A in more clearly (See Figure 5b).

This area was investigated in even more detail on both the front and back of the wafer. Figure 6a reveals the defect pattern on the wafer back surface, which is clearly the same as the pattern on the front (Figure 6b). In this case

the contamination on the wafer backside has diffused to the front surface. This is confirmed when analysing another wafer grown in the same reactor, but with a lower processing temperature (Figures 6c and 6d). The same contamination pattern as previously shown in Figure 6a is observed on the wafer backside (the spots are more defined because the impurities have diffused a shorter distance during the lower temperature) but not on the wafer front side, this is due to the lower processing temperature.

Defect and contamination analysis is also important for strained Si layers grown on SiGe relaxed substrates. In these structures it is important to measure the threading misfit dislocation density, because this can lead to degradation of device performance. Micro scans were performed on wafers containing strained Si layers grown on relaxed substrates. Micro scans show reveal dark spots aligned in orthogonal directions (see Figure 7). These localized areas of reduced signal lie along the <110> directions, and these features are attributed to threading dislocations (several threading defects are indicated by reference 201 in Figure 7). The faint horizontal and vertical lines are due to interfacial misfit dislocations in the underlying SiGe buffer layer. Defect etching results confirmed that the threading defect density detected by the invention correlated with the threading defect density measured using wet chemical etching.

The PL map would be processed and the average PL value calculated and then compared against a pre-determined value. This specified range would used to determine the wafer quality and therefore a go-no go process control procedure created. This procedure is illustrated graphically in Figure 8.

By setting up the specified range it is possible then to associate this range to any colour or grey-scale pattern and prepare a corresponding image. An example is illustrated in Figure 9. In the example wafer map the dark areas

show areas outside the specified range. This simple coding can be used to illustrate the variation in the wafer quality.

After the wafer quality has been investigated using the average PL signal level, further measurements can be recorded with higher resolution on wafers that have failed the specification. This will allow one to inspect the spatial variation in more detail, which may give a clearer indication of the source of the contamination (e.g. poor surface polishing or incomplete cleaning). Also the wafers could be further analysed to determine the type of defect present, for example using TXRF to identify any impurity.

To identify the source of contamination the front surface the back surface of the wafer can both be recorded. By comparison of the wafer maps, it will be apparent if the contamination originated on the wafer back surface. Then further action can be taken to prevent cross contamination to other process equipment of metrology tools.

Thus in accordance with the invention the photoluminescence tool is used as a rapid process control tool to determine wafer quality. Wafer maps are obtained and the measured PL response numerically analysed to provide a quality metric, in that a deviation of the photoluminescence response from predetermined parameters known to be associated with a semiconductor structure of satisfactory quality is used as the basis of a quality control decision.

In the basic example given this can simply be a comparison of mean response over the whole area. However in general contamination can be a very localised and the average PL signal (averaged over all measured pixels in the wafer map) may not a reliable indication of such contamination. If wafer map

is sub-divided using a 2D grid, then analysed using average PL, very localised signals could be detected.

After a wafer map has been recorded a virtual grid may be applied and displayed on top of the wafer map using suitable software. This can be used to perform the analysis. A local area analysis also allows better location of problem sites in the structure. For example the grid elements that have failed may be indicated, a micro scan can be launched at the same location as the grid element to allows the area of interest to be inspected in more detail, and a report of the failed elements in the wafer map analysis can be exported in suitable format.

The local grid method is not restricted to a numerical analysis based on mean values. Any suitable pre-defined parameters, including average intensity, PL min, Max, Standard deviation and baseline) can be used to determine regions of contamination. The PL signal baseline method can be a more useful parameter to use because the variation in signal across is not uniform wafer. This technique is explained below.

A typical wafer map is shown in figure 7a with an associated histogram of PL intensity in Figure 7b.

Contamination is detected in the wafer map by the deviation from the baseline value and limits can be set. However, the PL average value in this wafer map is modified by the contamination. Whereas the value to be used should represent the signal level for an uncontaminated wafer. The peak value shown in Figure 8 represents the true PL value of a non-contaminated wafer. Modifying the baseline function to have a peak value would allow the customer to accurately track the contamination and with more sensitivity.

A suitable algorithm involves the following steps:

1. To define peak value as maximum value in histogram and use this for baseline
2. Search data for peak value.
3. Then calculate ±70% of maximum value (user defined) then re-define the peak maximum as the center position of these points.
4. Then calculate precise value of peak maximum and then define PL level.
5. Also allow user to input typical baseline value form uncontaminated wafer, this will help if there are two peaks of equal intensity.

The baseline of the wafer is the PL value that corresponds to the maximum number of points.

The baseline variation is defined by the following relationship:

Baseline variation = PL value – baseline

The PL value is the AVG PL of each element of the grid. The baseline variation must be measured for each element.

CLAIMS

1. A method of quality screening silicon germanium epilayers by measuring defects and contamination therein comprises the steps of:
growing a silicon germanium layer epitaxially on a suitable substrate;
exposing the surface of the silicon germanium layer to at least one high-intensity beam of light from a suitable light source, and collecting photoluminescence (PL) produced by excitation of the silicon germanium layer by the light beam;
making an analysis of the collected photoluminescence signal and using that analysis as the basis for a quality classification of the suitability of the semiconductor for further processing.

2. A method in accordance with claim 1 wherein the quality classification step comprises:
determining an average photoluminescence intensity emitted across the area of the structure or subregions thereof;
comparing the average with a predetermined acceptable specification range of photoluminescence;
making a quality classification of the semiconductor structure based thereon.

3. A method in accordance with claim 1 or claim 2 wherein the quality classification step comprises rejecting or selecting for remedial action a grown silicon germanium layer exhibiting a photoluminescence response outside a predetermined acceptable specification range.

4. A method in accordance with any preceding claim applied as a quality control metric for silicon germanium epilayers intended for device fabrication thereupon, comprising the successive monitoring of a

successive series of grown layers in the manner above described, passing a layer exhibiting a photoluminescence response within a predetermined acceptable specification onto the next device fabrication stage, rejecting a layer exhibiting a photoluminescence response outside a predetermined acceptable specification from the next device fabrication stage.

5. A method in accordance with any preceding claim wherein the beam power and/or wavelength and/or spot size of the light beam is so controlled as to collect near-surface PL information from the upper 12 μm of the semiconductor structure.

6. A method in accordance with claim 5 wherein the light beam is so controlled as to collect near-surface PL information from the upper 1 μm of the semiconductor structure.

7. A method in accordance with any preceding claim wherein the PL response is obtained at around room temperature.

8. A method in accordance with any preceding claim wherein the light source is a high-intensity laser.

9. A method in accordance with claim 8 wherein the laser has a small probing volume with spot size 0.1 to 20μm, ideally 2 to 5μm, and with a peak or average power density of between 10^4 to 10^9 watts/cm^2.

10. A method in accordance with claim 8 or 9 wherein a pulsed laser excitation source is used and luminescence data is measured and/or the luminescence images collected as a function of time.

11. A method in accordance with any preceding claim further comprising the step of using the collected PL signals to generate a spatially resolved map of PL signals across the surface of the SiGe layer under test, and in particular to generate a spatially resolved image of those signals.

12. A method in accordance with claim 11 further comprising the step of storing the spatially resolved PL map on suitable data storage means and/or transmitting digitised data derived from the spatially resolved map through suitable processing means for onward processing.

13. A method in accordance with claim 11 or 12 further comprising the step of displaying any generated PL image on suitable display means.

14. A method in accordance with one of claims 11 to 13 further comprising the steps of using the spatially resolved map to identify the general location of a defect in the SiGe layer, and further analysing the layer structure in the identified location using a specific analysis technique capable of characterising any defects.

15. A method in accordance with claim 14 wherein the specific analysis step comprises performance of a micro scan to reveal individual stacking faults and like structural defects.

16. An apparatus for quality screening silicon germanium epilayers by measuring defects and contamination therein comprises a test device comprising a high intensity light source; means to focus a high intensity beam of light from the light source onto a surface of the silicon germanium layer under test; collection means to collect photoluminescence data from across the surface of the layer under test produced by excitation of the semiconductor structure by the light beam;

analysis means to process and numerically analyse the collected data; a comparator to compare the results of the analysis with predetermined acceptable specification parameters, and to accept or reject the structure determined by whether the photoluminescence signal falls within the predetermined acceptable specification.

17. An apparatus in accordance with claim 16 further comprising a means to grow an epitaxial silicon germanium layer on a suitable substrate, such as a chemical vapour deposition epitaxial reactor, in conjunction with a test device as above to test the as grown silicon germanium layer.

18. An apparatus in accordance with claim 16 or 17 further comprising transfer means to sequentially transfer grown layers from the reactor to the test device as part of a process control system.

19. An apparatus in accordance with one of claims 16 to 18 incorporated as part of a production line and including transfer means adapted to transfer the structure to a particular further processing stage determined by whether the photoluminescence signal falls within the predetermined acceptable specification range.

20. An apparatus in accordance with claim 19 wherein the transfer means is adapted to transfer a structure exhibiting a photoluminescence response within the predetermined acceptable specification range of photoluminescence on to the next device fabrication stage, and to reject a structure exhibiting a photoluminescence response outside the predetermined acceptable specification range of photoluminescence.

21. An apparatus in accordance with one of claims 16 to 20 wherein the beam power and/or wavelength and/or spot size of the light beam is so

controlled that the apparatus is adapted to generate and collect near-surface PL information from the upper 12 μm of the semiconductor structure.

22. An apparatus in accordance with one of claims 16 to 20 wherein the beam power and/or wavelength and/or spot size of the light beam is so controlled that the apparatus is adapted to generate and collect near-surface PL information from the upper 1 μm of the semiconductor structure.

23. An apparatus in accordance with one of claims 16 to 22 wherein the light source is a high-intensity laser.

24. An apparatus in accordance with claim 23 wherein the laser has a small probing volume with spot size 0.1 to 20μm, ideally 2 to 5μm, and with a peak or average power density of between 10^4 to 10^9 watts/cm^2.

25. An apparatus in accordance with one of claims 16 to 23 further comprising means to resolve the collected PL data into a spatially resolved PL map across the area of the semiconductor structure.

26. An apparatus in accordance with claim 25 further comprising means to convert the resolved data into a PL image and/or image/data storage means to store the map/image, and in particular to store successive map/images for future comparison, and/or means to transmit the map/image to a suitable remote data processor and/or image display means such as a visual display screen to display an image and/or related data to a user.

27. An apparatus in accordance with claim 24 or 25 further comprising a micro scanner to characterise defects spatially identified by the PL map.

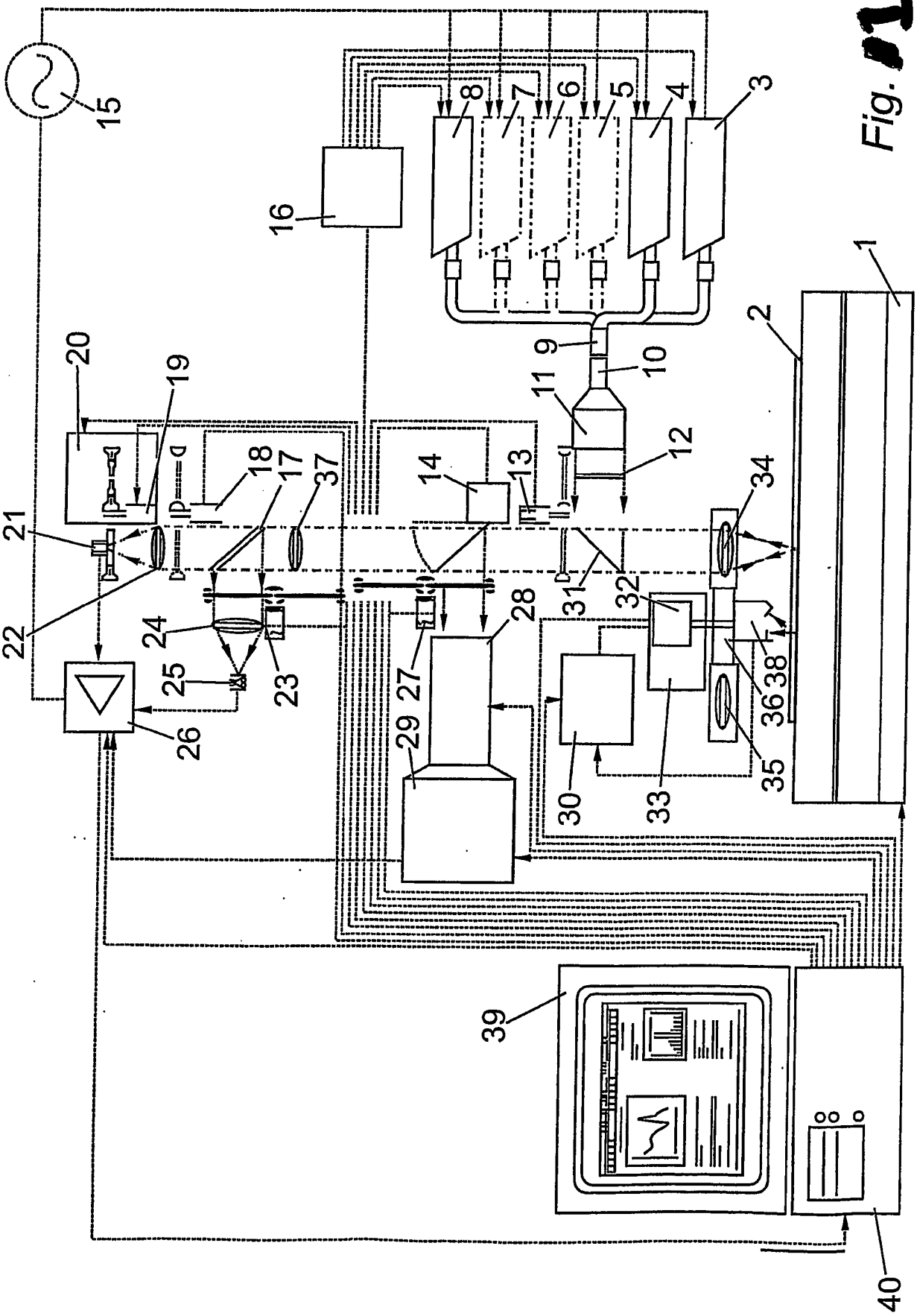
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Fig. 1

Figure 2

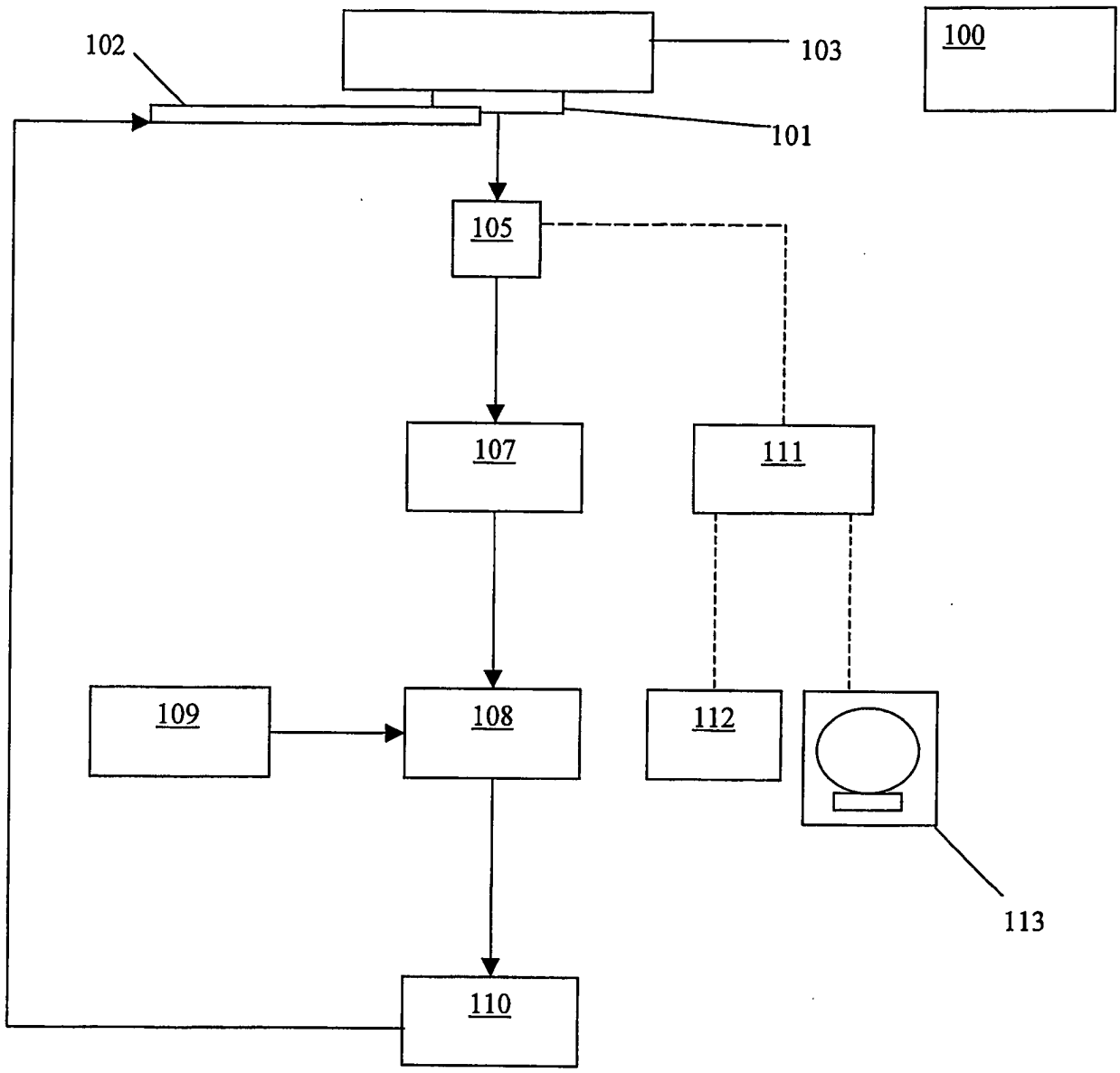


Figure 3a

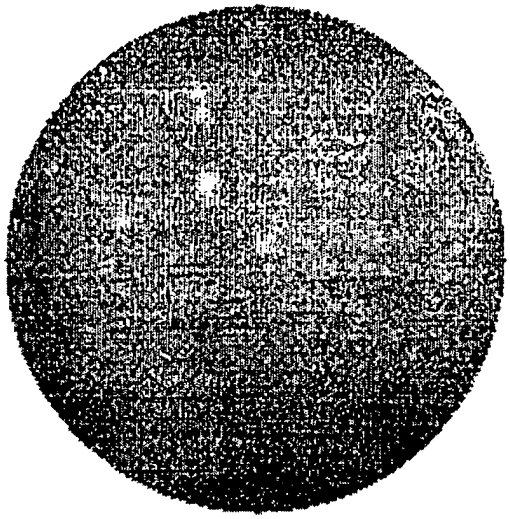


Figure 3b

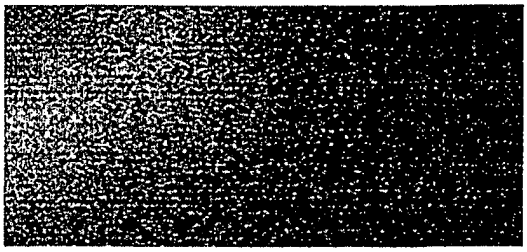


Figure 4a

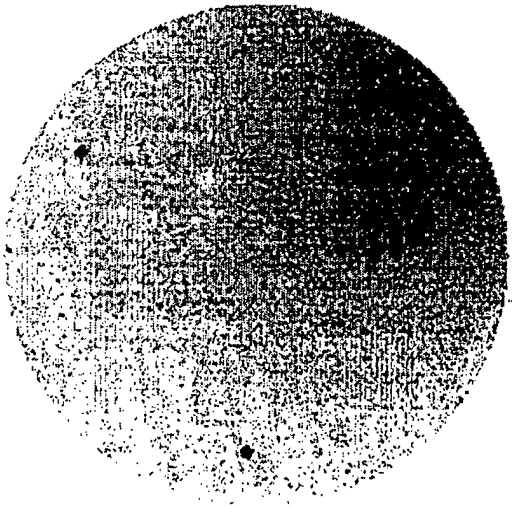


Figure 4b

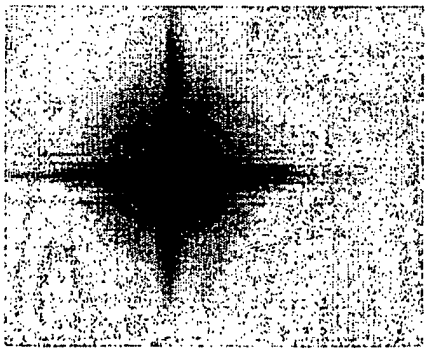


Figure 5a

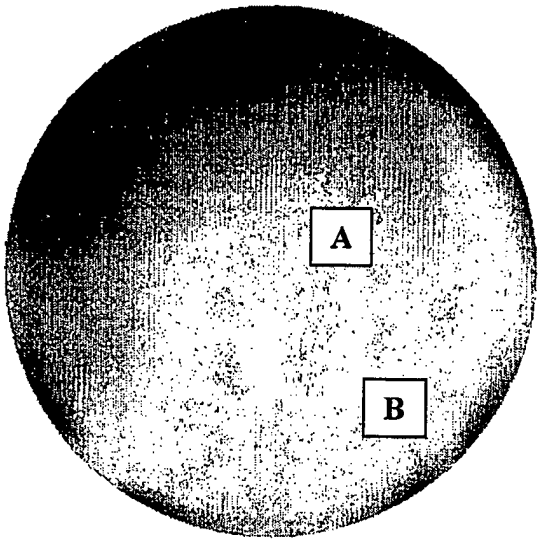


Figure 5b

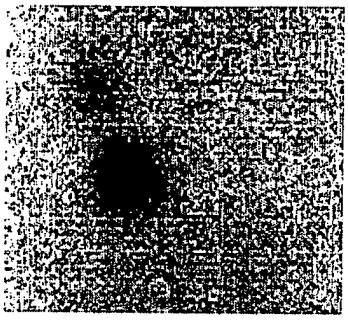


Figure 6a

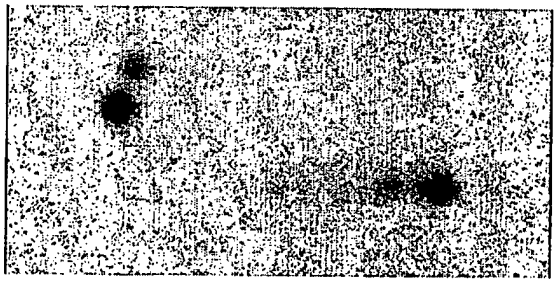


Figure 6b

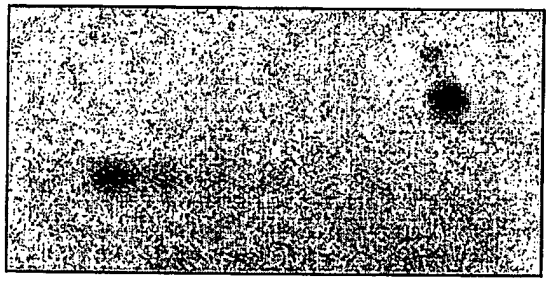


Figure 6c

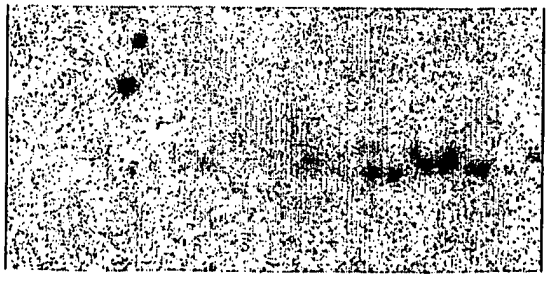


Figure 6d

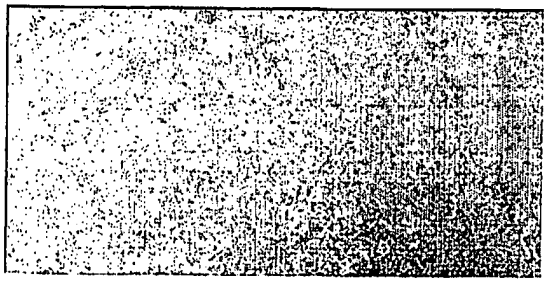


Figure 7

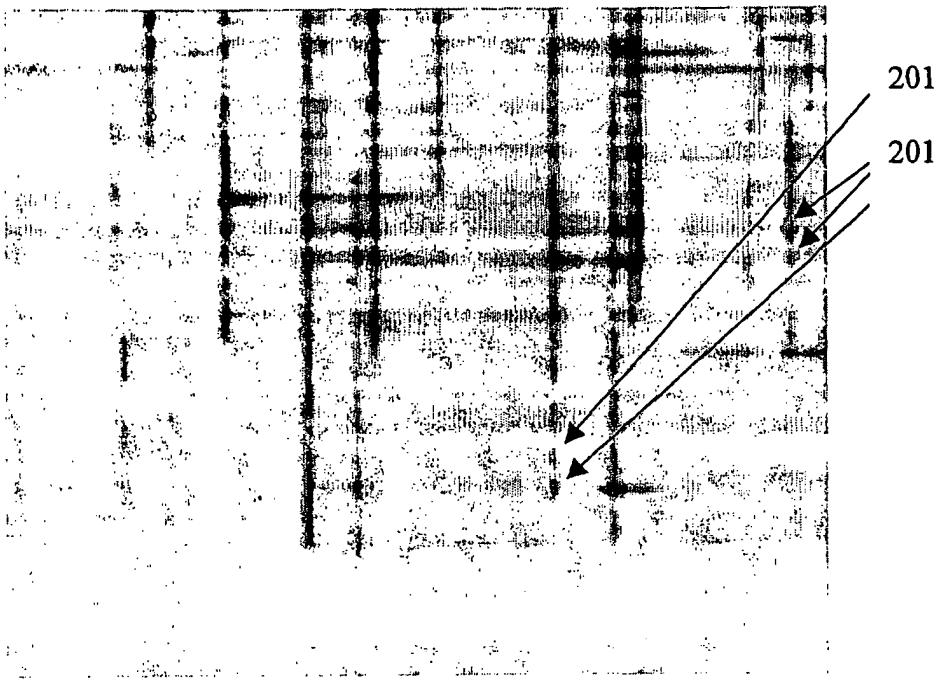


Figure 8

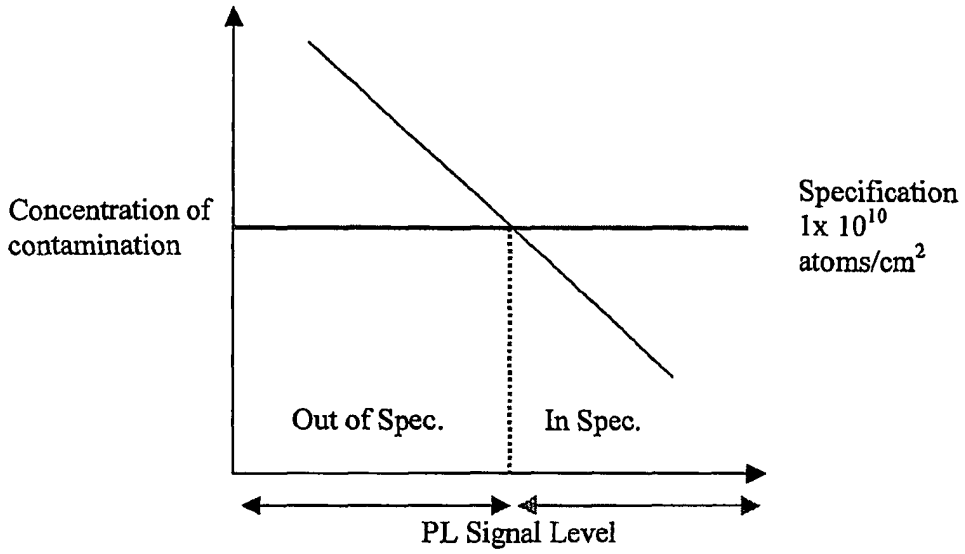
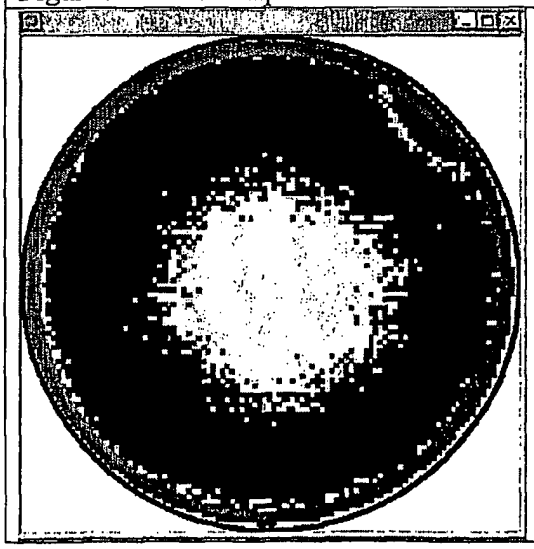


Figure 9. Wafer Map



PL Color Histogram Representation

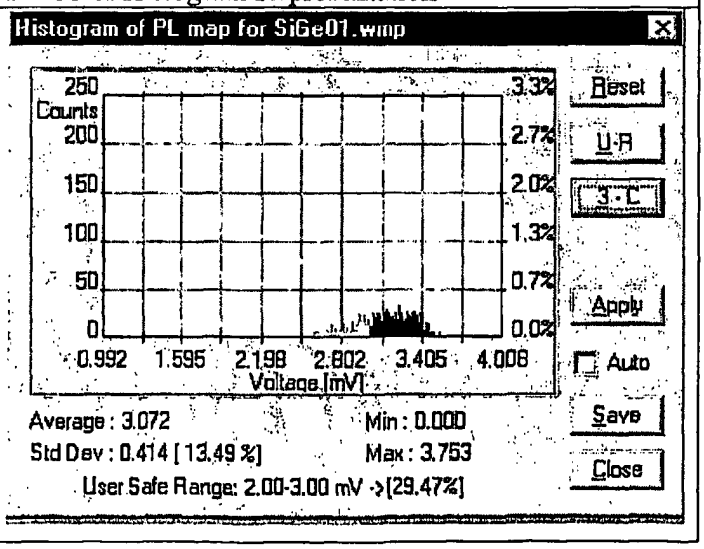


Figure 10a wafer map

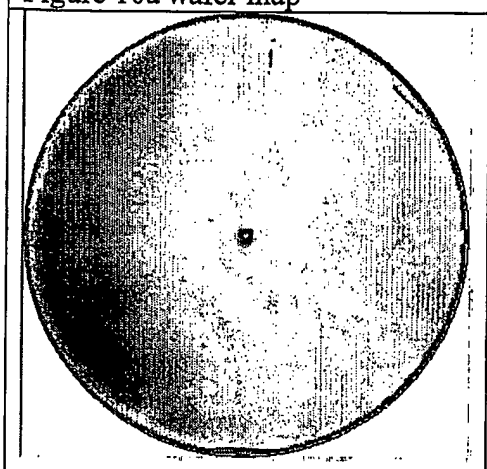


Figure 10b

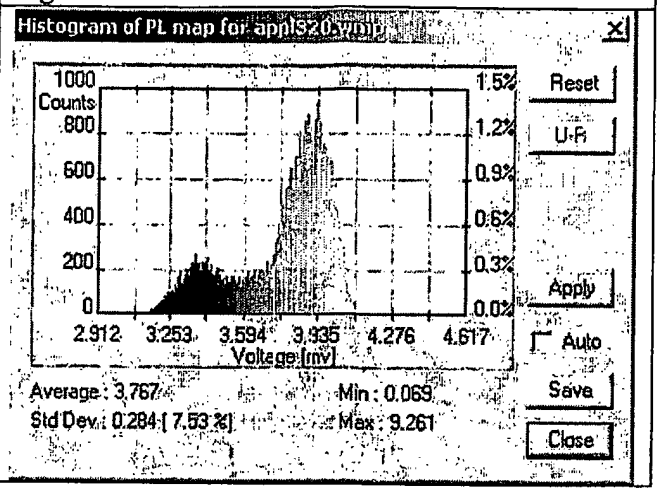
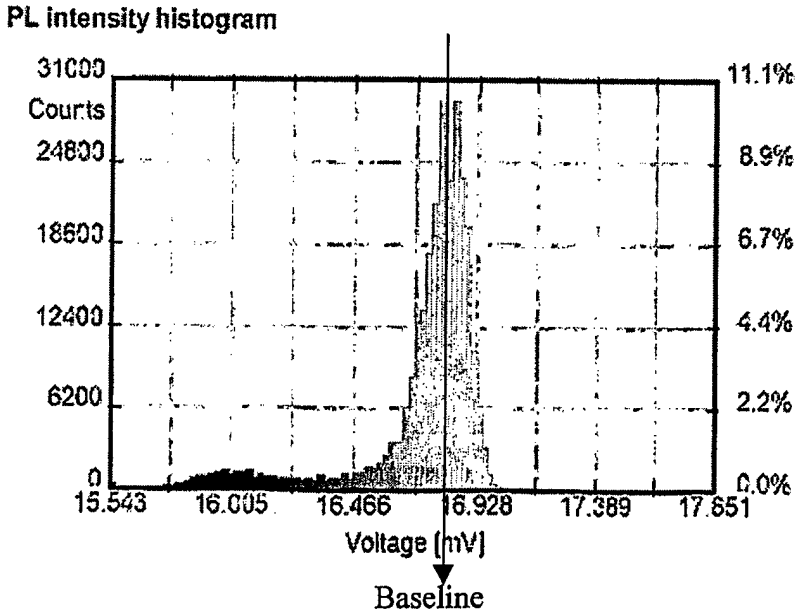


Figure 11



INTERNATIONAL SEARCH REPORT

Inte ··· ıal Application No
PC.,.B 03/03022

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G01N21/64 G01N21/95 H01L21/66

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G01N H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	HIGGS V: "Characterization of Si, SiGe and SOI Structures using Photoluminescence" MAT.RES.SOC.SYMP.PROC., vol. 588, 2000, pages 129-140, XP009017743 cited in the application the whole document ---	1-23, 25-27
Y	WO 98 11425 A (BIO RAD MICROMEASUREMENTS LTD ;MAYES IAN CHRISTOPHER (GB); HIGGS V) 19 March 1998 (1998-03-19) cited in the application the whole document ---	1,5-16, 18-20, 23-27
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[X] Further documents are listed in the continuation of box C. [X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 September 2003	29/10/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Meyer, F

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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X	WESTRATE S ET AL: "PHOTOLUMINESCENCE MAPPING DETECTS CU CONTAMINATION IN SI WAFERS" SOLID STATE TECHNOLOGY, COWAN PUBL.CORP. WASHINGTON, US, vol. 45, no. 2, February 2002 (2002-02), pages 57-58, XP001092608 ISSN: 0038-111X	16, 21-23, 25-27
Y	the whole document	1,2,5-8, 11-15, 18-20
Y	HIGGS V ET AL: "Photoluminescence characterization of defects in Si and SiGe structures" EXTENDED DEFECTS IN SEMICONDUCTORS 2000, BRIGHTON, UK, 18-22 JULY 2000, vol. 12, no. 49, pages 10105-10121, XP002255686 Journal of Physics: Condensed Matter, 11 Dec. 2000, IOP Publishing, UK ISSN: 0953-8984 the whole document	1-16, 18-23, 25-27
Y	WO 99 44231 A (DAVIDSON BRIAN ;SHIN ETSU HANDOTAI EUROP LIMIT (GB)) 2 September 1999 (1999-09-02) abstract page 2, line 1-25; figure 1	16-27
Y	US 4 571 685 A (KAMOSHIDA MOTOTAKA) 18 February 1986 (1986-02-18) abstract column 5, line 24-34 column 7, line 48 -column 9, line 42 figure 9	16-27

INTERNATIONAL SEARCH REPORT

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Inte nal Application No
PC., GB 03/03022

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